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Title: Simon: Programmiersprachen (26.10.2012)

Date: Fri Oct 26 10:19:14 CEST 2012

Duration: 73:04 min

Pages: 70

TECHNISCHE UNIVERSITÄT MÜNCHEN
FAKULTÄT FÜR INFORMATIK

Programming Languages

Concurrency: Memory Consistency

Dr. Axel Simon and Dr. Michael Petter
Winter term 2012

Need for Concurrency

Consider two processors:

- in 1997 the *Pentium P55C* had 4.5M transistors
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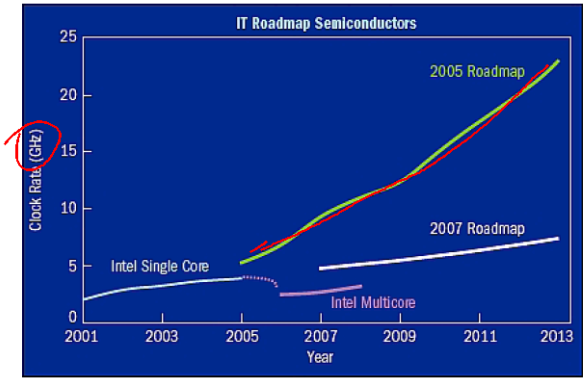
However:

- most programs are not inherently parallel
  - ⇝ parallelizing a program is between difficult and impossible
- correctly communicating between different cores is challenging
  - ⇝ correctness of concurrent communication is very hard
  - low-level aspects: locking algorithms must be correct
  - high-level aspects: program may deadlock
- a program on n cores runs $m \ll n$ times faster
  - ⇝ all effort is voided if program runs no faster
  - distributing work load is application specific

The free lunch is over

Single processors cannot be made much faster due to physical limitations.



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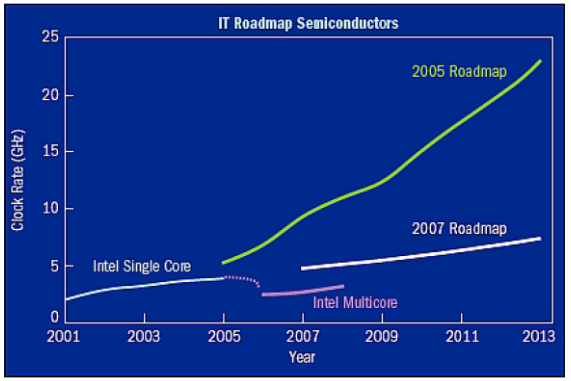

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But Moore's law still holds for the number of transistors:

- they double every 18 months for the foreseeable future
- may translate into doubling the number of cores
- programs have to become parallel

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Concurrency for the Programmer

How is concurrency exposed in a programming language?

1. spawning of new concurrent computations
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Communication can happen in many ways:

- communication via shared memory *(this lecture)*
- atomic transactions on shared memory
- message passing

Learning Outcomes

1. Happened-before Partial Order
2. Sequential Consistency
3. The MESI Cache Model
4. Weak Consistency
5. Memory Barriers

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Communication between Cores

We consider the concurrent execution of these functions:

Thread A

```
void foo(void) {
  a = 1;
  b = 1;
}
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Thread B

```
void bar(void) {
  while (b == 0) {};
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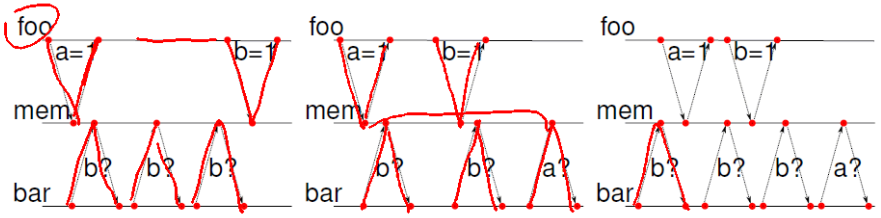
- B should see `b` go to one before executing the `assert` statement
- the `assert` statement should always hold
- here the code is *correct* if the `assert` holds

⇝ correctness means: writing a one to `a` *happens before* reading a one in `b`

Strict Consistency

Assuming `foo` and `bar` are started on two cores operating in lock-step.
Then *one* of the following may happen:



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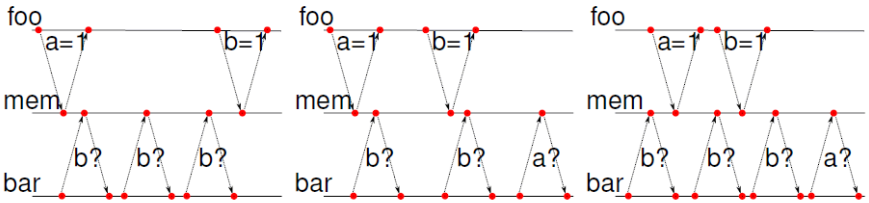

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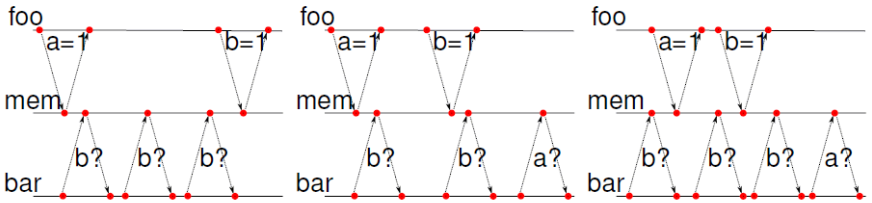

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⇝ strict consistency is too strong to be realistic
⇝ state correctness in terms of what event *may* happen before another one

Events in a Distributed System

A process as a series of events [Lamport(1978)]: Given a distributed system of processes $P, \ldots$, each process P consists of events $p_1, p_2, \ldots$.

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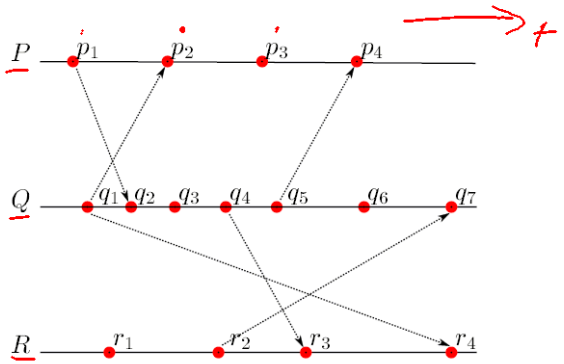

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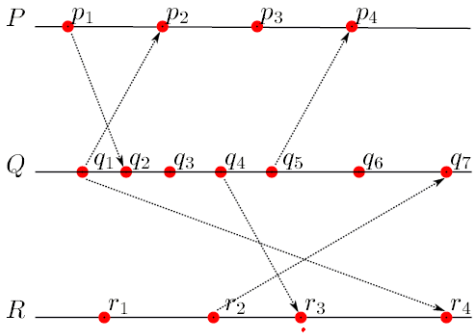

- event p_i in process P *happened before* p_{i+1}
- if p_i is an event that sends a message to Q then there is some event q_j in Q that receives this message and p_i *happened before* q_j

The Happened-Before Relation

Definition

If an event p *happened before* an event q then $p \rightarrow q$.

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Memory Consistency | Happened-Before Relation | 8 / 35

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Note: a strict partial order $\prec$ differs from a (non-strict) partial order $\preceq$ due to:

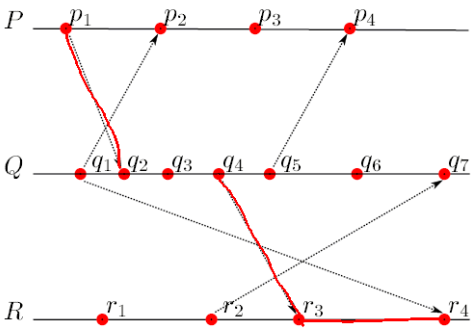
strict partial order	non-strict partial order
irreflexive $\neg(p \prec p)$	reflexive $p \preceq p$
asymmetric $p \prec q \iff \neg(q \prec p)$	antisymmetric $p \preceq q \wedge q \preceq p$ implies $p = q$

Concurrency

Let $a \not\to b$ abbreviate $\neg(a \to b)$.

Definition

Two distinct events p and q are said to be *concurrent* if $p \not\to q$ and $q \not\to p$.



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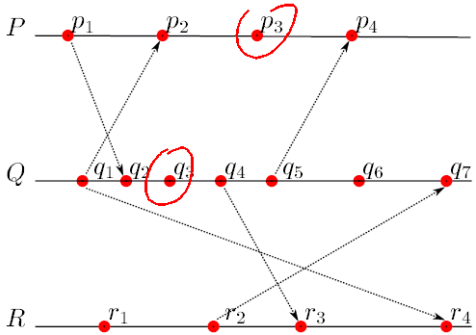

- $p_1 \to r_4$ in the example
- p_3 and q_3 are, in fact, concurrent since $p_3 \not\to q_3$ and $q_3 \not\to p_3$

Ordering

Let C be a *logical clock* that assigns a time-stamp $C(p)$ to each event p.

Definition (Clock Condition)

C satisfies the *clock condition* if for any events $p \to q$ then $C(p) < C(q)$.

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For a distributes system the *clock condition* holds iff:

1. if p_i and p_j are events of P and $p_i \rightarrow p_j$ then $C(p_i) < C(p_j)$
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The *set* of C that satisfy the clock condition are exactly the *set* of executions possible in the system.
$\rightsquigarrow$ use the process model and $\rightarrow$ to define better consistency model

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Note: there is no observable change if calculations on different memory locations can happen in parallel.

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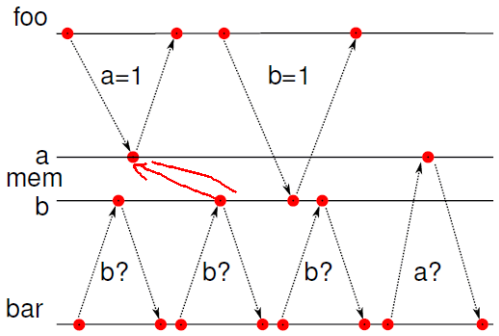

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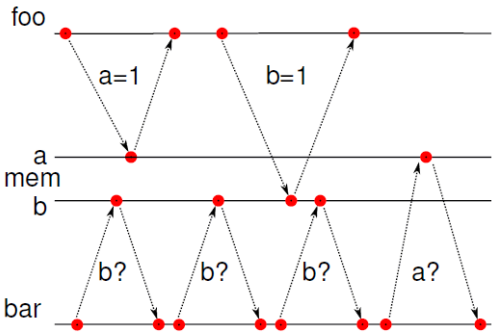

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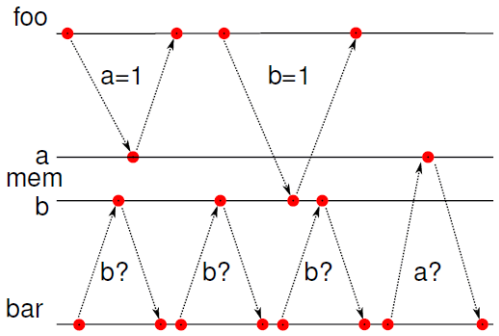

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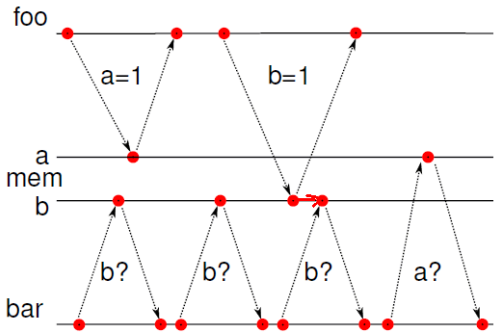

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Not a realistic model for modern hardware with out-of-order execution:

- memory accesses are only sequentially consistent from the point of view of the processor executing them
- what other processors see is determined by the complex protocol of the caches

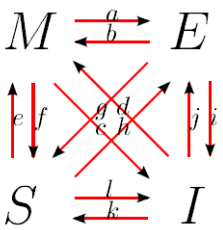
⇝ need to understand how caches work

The MESI Protocol: States

Processors (and also: GPUs, intelligent I/O devices) use caches to avoid a costly round-trip to RAM for every memory access.

- programs often access the same memory area repeatedly (e.g. stack)
- keeping a local mirror image of certain memory regions requires bookkeeping about who has the latest copy

Each cache line is in one of the states M, E, S, I:



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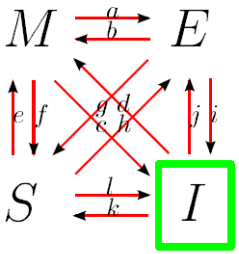

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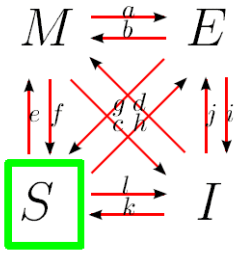

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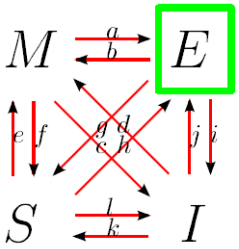

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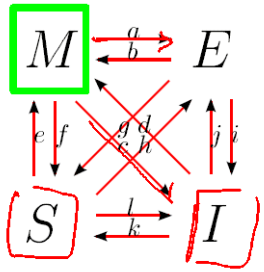

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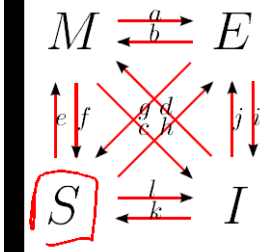

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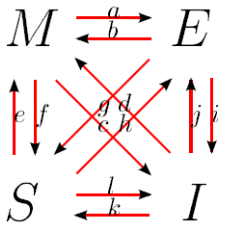
$\rightsquigarrow$ the state of cache lines is kept consistent by sending *messages*

The MESI Protocol: Messages

Moving data between caches is coordinated by sending messages [McKenny(2010)]:

- *Read:* sent if CPU needs to read from an address



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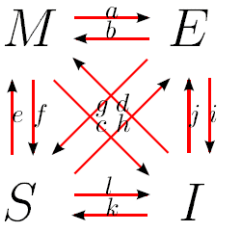

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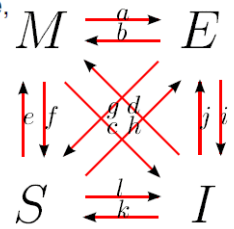
- *Invalidate:* asks others to evict a cache line



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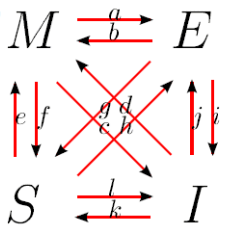

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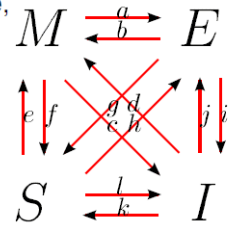

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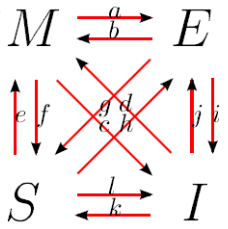

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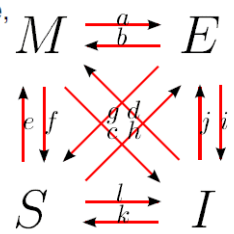


Additional *store* and *read* messages are transmitted to main memory.

MESI Example (I)

Thread A

```
a = 1;     // A.1
b = 1;     // A.2
```

Thread B

```
while (b == 0) {};   // B.1
assert(a == 1);      // B.2
```

state-ment	CPU A a	CPU A b	CPU B a	CPU B b	RAM a	RAM b	message
A.1	- I	- I	- I	- I	0	0	
	- I	- I	- I	- I	0	0	*read invalidate* of a from CPU A
	- I	- I	- I	- I	0	0	*invalidate ack.* of a from CPU B
	1 M	- I	- I	- I	0	0	*read response* of a=0 from RAM
B.1	1 M	- I	- I	- I	0	0	*read* of b from CPU B
	1 M	- I	- I	- I	0	0	*read response* with b=0 from RAM
	1 M	- I	- I	0 E	0	0	
B.1	1 M	- I	- I	0 E	0	0	
A.2	1 M	- I	- I	0 E	0	0	*read invalidate* of b from CPU A
	1 M	- I	- I	- I	0	0	*invalidate ack.* of b from CPU B
	1 M	- I	- I	- I	0	0	*read response* of b=0 from CPU B
	1 M	1 M	- I	- I	0	0	

MESI Example (II)

Thread A

```
a = 1;     // A.1
b = 1;     // A.2
```

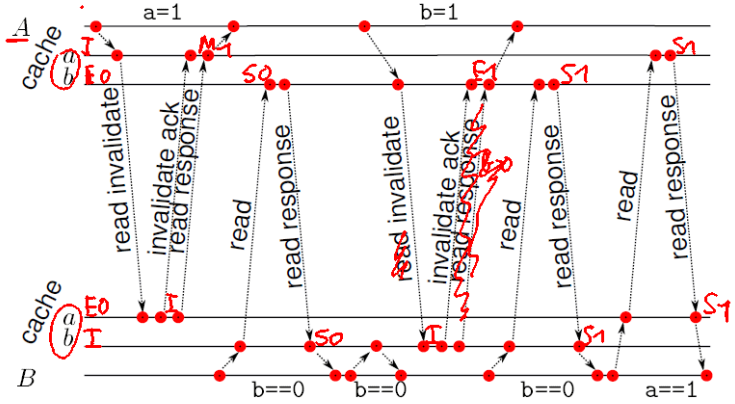
Thread B

```
while (b == 0) {};   // B.1
assert(a == 1);      // B.2
```

state-ment	CPU A a	CPU A b	CPU B a	CPU B b	RAM a	RAM b	message
B.1	1 M	1 M	- I	- I	0	0	
	1 M	1 M	- I	- I	0	0	*read* of b from CPU B
B.2	1 M	1 S	- I	1 S	0	0	*read response* of b=1 from CPU A
	1 M	1 S	- I	1 S	0	0	*read* of a from CPU B
	1 S	1 S	1 S	1 S	0	0	*read response* of a=1 from CPU A
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
A.1	1 S	1 S	1 S	1 S	0	0	
	1 S	1 S	- I	1 S	0	0	*invalidate* of a from CPU A
	1 M	1 S	- I	1 S	0	0	*invalidate ack.* of a from CPU B

MESI Example: Happened Before Model

Idea: each cache line one process, model each message



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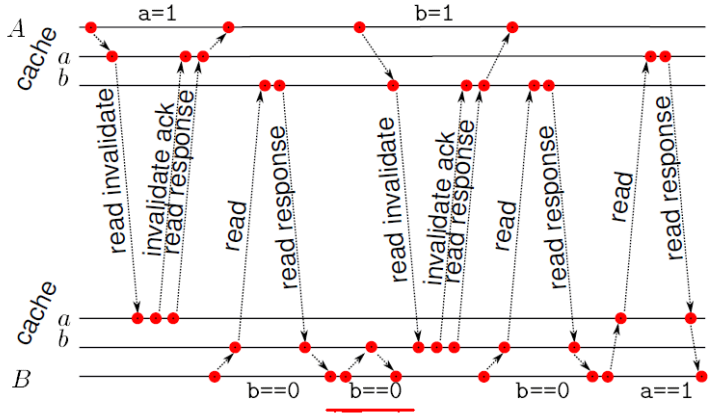

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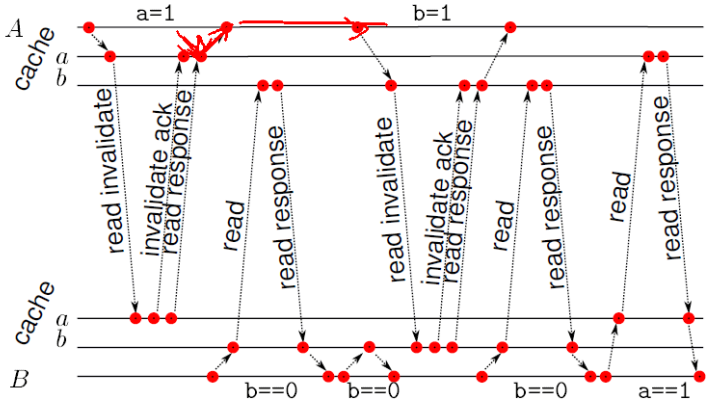

Observations:

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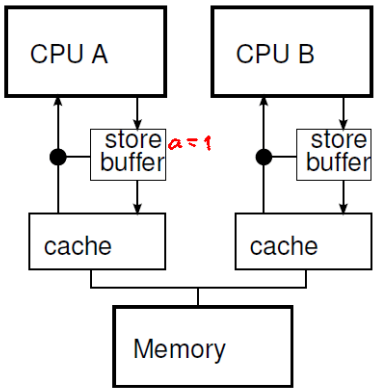
- second execution of test `b==0` stays within cache ⇝ no traffic
- writes always stall ⇝ CPU A should continue executing after $a = 1$

Store Buffers

Goal: continue execution after write operation



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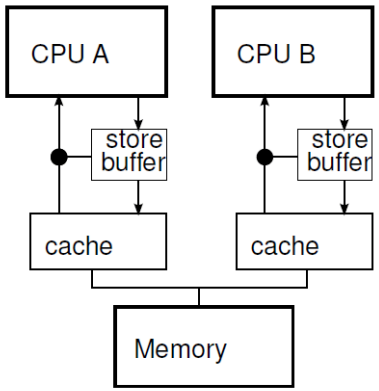

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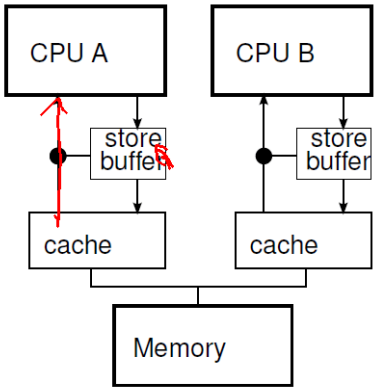

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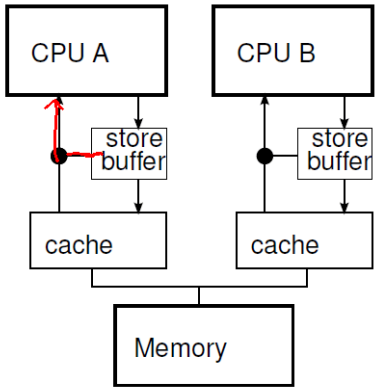

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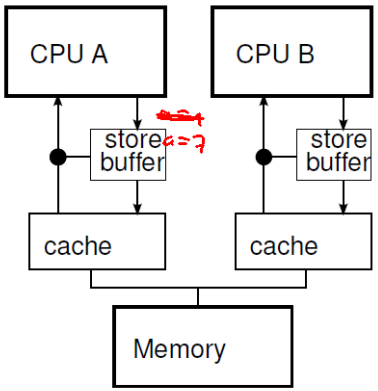

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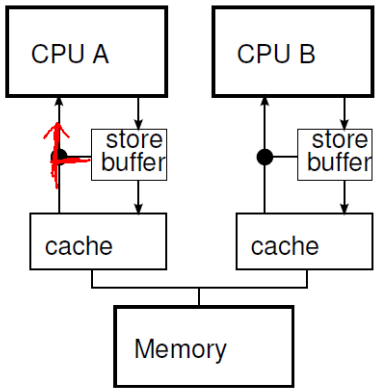

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What about sequential consistency for the whole system?

Happened-Before Model for Store Buffers

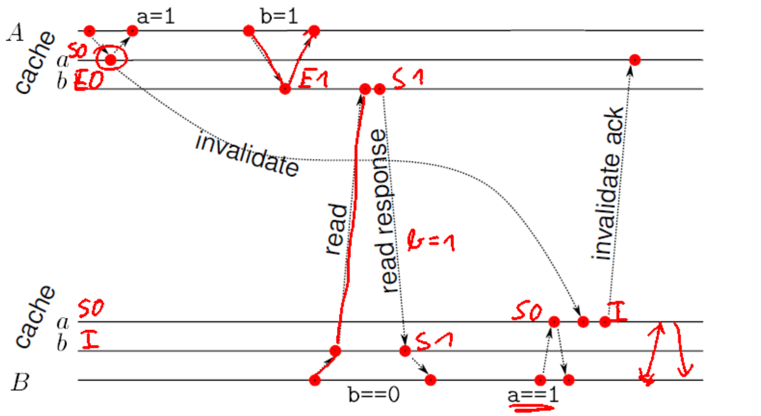
Thread A

```
a = 1;
b = 1;
```

Thread B

```
while (b == 0) {};
assert(a == 1);
```

Assume cache A contains: a: S0, b: E0, cache B contains: a: S0, b: I



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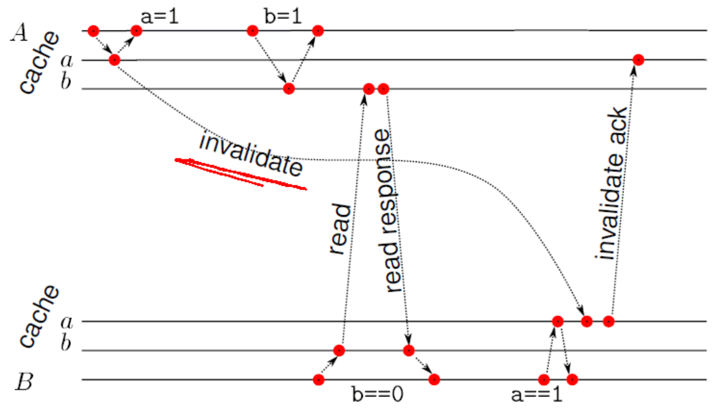

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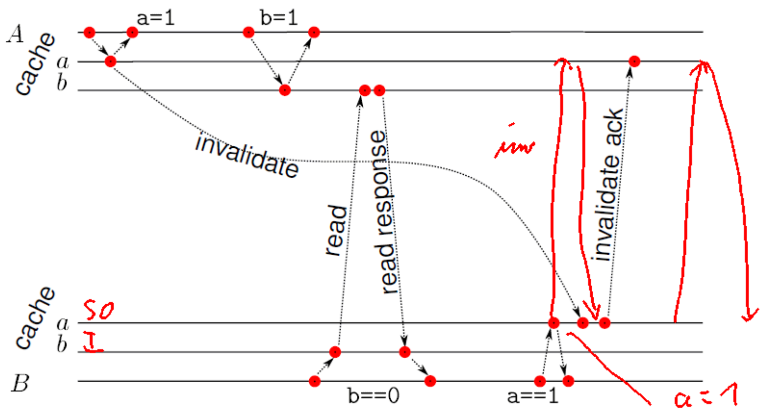

Explicit Synchronisation: Write Barrier

Overtaking of messages *is desirable* and should not be prohibited in general.

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- Intel x86 CPUs provide the `sfence` instruction
- a write barrier marks all current store operations in the store buffer
- the next store operation is only executed when all marked stores in the buffer have completed

Happened-Before Model for Write Fences

Thread A

```
a = 1;
sfence();
b = 1;
```

Thread B

```
while (b == 0) {};
assert(a == 1);
```

Assume cache A contains: a: S0, b: E0, cache B contains: a: S0, b: I